CLAIMS

What is claimed is:

1. An embedded DRAM memory cell, comprising:

an access transistor, the access transistor comprising:

a source and a drain within a substrate, and having a channel region therebetween; and

a gate dielectric and a gate electrode overlying the channel region, the gate electrode forming a portion of a word line associated with the DRAM memory cell;

the access transistor covered by a first insulating layer;

a bit line contact pillar extending through the first insulating layer and contacting the drain of the access transistor, the bit line contact pillar composed of a contact conductive material;

a three dimensional capacitor structure comprising:

a storage plate comprising a storage contact pillar residing within a trench formed in the first insulating layer, and coupled to the source of the access transistor, and laterally spaced away from a side wall of the trench; and

a capacitor dielectric layer overlaying the trench and the storage contact pillar within the trench; and

a ground plate overlying the capacitor dielectric layer;

a second insulating layer overlying the access transistor, and having a first opening overlying the bit line contact pillar and a second opening overlying the trench; and

a conductive material within the first and second openings, respectively, wherein the conductive material within the first opening comprises a bit line contact and the conductive material within the second opening comprises the ground plate of the three dimensional capacitor structure.

2. The memory cell of claim 1, wherein the capacitor further comprises an overlying insulating dielectric layer.

3. The memory cell of claim 1, wherein the capacitor comprises multiple storage contact pillars.

4. The memory cell of claim 1, wherein the contact conductive material and the conductive material comprise substantially one material.

5. The memory cell of claim 4, wherein the one material is selected from the group consisting of tungsten, copper, aluminum, and copper overlying a tantalum nitride barrier layer.

6. The memory cell of claim 1, wherein the storage contact pillar comprises the contact conductive material.

7. The memory cell of claim 1, wherein the capacitor dielectric layer of the capacitor comprises tantalum pentoxide.

8. The memory cell of claim 1, wherein the contact conductive material, and the conductive material comprise one of tungsten, copper, aluminum, and copper overlying a tantalum nitride barrier layer.

9. The memory cell of claim 1, wherein the first insulating layer covering the access transistor comprises a PMD layer.

10. The memory cell of claim 1, wherein the conductive material overlying the bit line contact pillar comprises an M1 layer.

11. The memory cell of claim 1, wherein the ground plate of the capacitor provides a structure which is continuous across adjoining cells and connects the adjoining cells.

12. The memory cell of claim 1, wherein the trench formed in the first insulating layer overlaps the transistor gate electrode.

13. An embedded DRAM memory cell, comprising:

an access transistor, the access transistor comprising:

a source and a drain within a substrate, and having a channel region therebetween; and

a gate dielectric and a gate electrode overlying the channel region, the gate electrode forming a portion of a word line associated with the DRAM memory cell;

the access transistor covered by a first insulating layer;

a bit line contact pillar extending through the first insulating layer and contacting the drain of the access transistor, the bit line contact pillar composed of a contact conductive material;

a three dimensional capacitor structure comprising:

a storage plate comprising a storage contact pillar residing within a trench formed in the first insulating layer, and coupled to the source of the access transistor, and laterally spaced away from a side wall of the trench; and

a capacitor dielectric layer overlaying the trench and the storage contact pillar within the trench and defining a ground plate region surrounding the storage contact pillar;

a conductive plate material residing in the ground plate region surrounding the storage contact pillar with the capacitor dielectric layer disposed therebetween, the conductive plate material forming a ground plate for the three dimensional capacitor structure;

a second insulating layer overlying the access transistor and the three dimensional capacitor structure, the second insulating layer having a first opening overlying the bit line contact pillar and a second opening overlying a portion of the ground plate; and

a conductive material within the first and second openings, respectively, wherein the conductive material within the first opening comprises a bit line contact and the conductive material within the second opening comprises a ground plate contact for the ground plate of the three dimensional capacitor structure.

14. The memory cell of claim 13, wherein the capacitor further comprises an overlying insulating dielectric layer.

15. The memory cell of claim 13, wherein the capacitor comprises multiple storage contact pillars.

16. The memory cell of claim 13, wherein the contact conductive material and the conductive material comprise substantially one material.

17. The memory cell of claim 16, wherein the one material is selected from the group consisting of tungsten, copper, aluminum, and copper overlying a tantalum nitride barrier layer.

18. The memory cell of claim 13, wherein the storage contact pillar comprises the contact conductive material.

19. The memory cell of claim 13, wherein the capacitor dielectric layer of the capacitor comprises tantalum pentoxide.

20. The memory cell of claim 13, wherein the contact conductive material, the conductive material and the conductive plate material comprise one of tungsten, copper, aluminum, and copper overlying a tantalum nitride barrier layer.

21. The memory cell of claim 13, wherein the first insulating layer covering the access transistor comprises a PMD layer.

22. The memory cell of claim 13, wherein the conductive material overlying the bit line contact pillar comprises an M1 layer.

23. The memory cell of claim 13, wherein one plate of the three dimensional capacitor comprises a laterally extending, non-linear pattern to increase capacitor surface area.

24. The memory cell of claim 13, wherein the memory cell has a portion of the storage contact pillar which extends into a region of the first insulating layer which is not removed, whereby structural strength of the cell is improved during processing.

25. The memory cell of claim 13, wherein the ground plate of the capacitor provides a structure which is continuous across adjoining cells and connects the adjoining cells.

26. The memory cell of claim 13, wherein the trench formed in the first insulating layer overlaps the transistor gate electrode.

27. An embedded DRAM memory cell, comprising:

an access transistor, the access transistor comprising:

a source and a drain within a substrate, and having a channel region therebetween; and

a gate dielectric and a gate electrode overlying the channel region, the gate electrode forming a portion of a word line associated with the DRAM memory cell;

the access transistor covered by a first insulating layer;

a bit line contact pillar extending through the first insulating layer and contacting the drain of the access transistor, the bit line contact pillar composed of a contact conductive material;

a storage contact pillar extending through the first insulating layer and contacting the source of the access transistor;

a three dimensional capacitor structure comprising:

an active region formed in the substrate and electrically isolated from the source and drain of the access transistor, the active region comprising a ground plate region of the capacitor structure;

a ground plate contact pillar residing within a trench formed in the first insulating layer, the ground plate contact pillar composed of the contact conductive material, and laterally spaced away from a side wall of the trench; and

a capacitor dielectric layer overlaying the trench and the ground plate contact pillar within the trench and defining a storage plate region between the sidewall of the trench and the ground plate contact pillar;

a conductive plate material residing in the storage plate region, the conductive plate material forming a storage plate of the capacitor structure;

a second insulating layer overlying the access transistor and the three dimensional capacitor structure, the second insulating layer having a first opening overlying the bit line contact pillar and a second opening overlying both the storage contact pillar and the storage plate; and

a conductive material within the first and second openings, wherein the conductive material within the first opening comprises a bit line contact and the conductive material within the second opening comprises an electrical

connection between the source of the access transistor and the storage plate of the capacitor structure.

28. The memory cell of claim 27, wherein the capacitor further comprises an overlying insulating dielectric layer.

29. The memory cell of claim 27, wherein the capacitor comprises multiple storage contact pillars.

30. The memory cell of claim 27, wherein the contact conductive material and the conductive material comprise substantially one material.

31. The memory cell of claim 30, wherein the one material is selected from the group consisting of tungsten, copper, aluminum, and copper overlying a tantalum nitride barrier layer.

32. The memory cell of claim 27, wherein the storage contact pillar comprises the contact conductive material.

33. The memory cell of claim 27, wherein the capacitor dielectric layer of the capacitor comprises tantalum pentoxide.

34. The memory cell of claim 27, wherein the contact conductive material, the conductive material and the conductive plate material comprise one of tungsten, copper, aluminum, and copper overlying a tantalum nitride barrier layer.

35. The memory cell of claim 27, wherein the first insulating layer covering the access transistor comprises a PMD layer.

36. The memory cell of claim 27, wherein the conductive material overlying the bit line contact pillar comprises an M1 layer.

37. The memory cell of claim 27, wherein one plate of the three dimensional capacitor comprises a laterally extending, non-linear pattern to increase capacitor surface area.

38. The memory cell of claim 27, wherein the ground plate contact pillar of the capacitor provides a structure which is continuous across adjoining cells and connects the adjoining cells.

39. The memory cell of claim 27, wherein the trench formed in the first insulating layer overlaps the transistor gate electrode.

40. The memory cell of claim 39, wherein the conductive material, deposited through an additional opening in the second insulating layer to the ground plate contact pillar, provides a contact to supply an electrical connection to the ground plate which is continuous across adjoining cells and connects the adjoining cells.

41. A method of forming a capacitor under bitline DRAM memory cell, comprising:

forming within a first insulating layer an access transistor for the memory cell comprising:

a source and a drain within a substrate, and having a channel region therebetween, the source, drain and the channel region each defining an active area of the substrate; and

a gate dielectric and a gate electrode overlying the channel region, the gate electrode forming a portion of a word line associated with the DRAM memory cell;

forming within the first insulating layer a bit line contact pillar of a contact conductive material extending through the first insulating layer and contacting the drain of the access transistor for electrical connection with a bit line;

forming within the first insulating a storage contact pillar of the contact conductive material extending through the first insulating layer and contacting the source of the access transistor for electrical connection with a memory cell capacitor;

forming a trench in the first insulating layer extending down toward the substrate, exposing a portion of the storage contact pillar operable as a storage plate of the memory cell capacitor;

depositing a capacitor dielectric layer over the trench, thereby covering the exposed portion of the storage contact pillar;

depositing a second insulating layer over the capacitor dielectric layer;

removing portions of the second insulating layer to expose an opening in the second insulating layer overlying the bit line contact pillar and to define a capacitor plate area associated with the trench;

removing portions of the capacitor dielectric layer to expose an opening in the capacitor dielectric layer overlying the bit line contact pillar for a contact to the bit line contact pillar; and

depositing and planarizing a conductive material layer over the capacitor dielectric layer in the trench capacitor plate area, and the bit line contact pillar, wherein the conductive material layer in the trench capacitor plate area is operable as a ground plate of the memory cell capacitor.

42. The method of claim 41, further comprising:

depositing and planarizing a layer of conductive capacitor plate material over the capacitor dielectric layer in the trench capacitor plate area.

43. The method of claim 41, wherein the conductive material layer within the first and second openings is deposited during an M1 conductive material layer deposition.

44. The method of claim 41, wherein the forming a trench in the first insulating layer extends down to about the uppermost surface of the substrate.

45. A method of forming a capacitor under bitline DRAM memory cell, comprising:

forming within a first insulating layer an access transistor for the memory cell comprising:

a source and a drain within a substrate, and having a channel region therebetween, the source, drain and the channel region each defining an active area of the substrate; and

a gate dielectric and a gate electrode overlying the channel region, the gate electrode forming a portion of a word line associated with the DRAM memory cell;

forming within the first insulating layer a bit line contact pillar of a contact conductive material extending through the first insulating layer and contacting the drain of the access transistor for electrical connection with a bit line;

forming within the first insulating layer a storage contact pillar of the contact conductive material extending through the first insulating layer and contacting the source of the access transistor for electrical connection with a memory cell capacitor;

forming a trench in the first insulating layer extending down toward the substrate, exposing a portion of the storage contact pillar operable as a storage plate of the memory cell capacitor;

depositing a capacitor dielectric layer over the trench, thereby covering the exposed portion of the storage contact pillar;

depositing and planarizing a layer of conductive capacitor plate material over the capacitor dielectric layer in the trench defining a ground plate of the memory cell capacitor;

depositing and planarizing a second insulating layer over the capacitor dielectric layer;

removing portions of the second insulating layer to expose an opening in the second insulating layer overlying the bit line contact pillar and an opening overlying a portion of the capacitor plate material used as the ground plate; and

depositing and planarizing a conductive material layer through the openings in the second insulating layer for contact to the bit line contact pillar and a portion of the capacitor plate material operable as the ground plate of the memory cell capacitor.

46. The method of claim 45, wherein the forming a trench in the first insulating layer extends down to about the uppermost surface of the substrate.

47. A method of forming a capacitor under bitline DRAM memory cell, comprising:

forming within a first insulating layer an access transistor for the memory cell comprising:

a source and a drain within a substrate, and having a channel region therebetween, the source, drain and the channel region each defining an active area of the substrate; and

a gate dielectric and a gate electrode overlying the channel region, the gate electrode forming a portion of a word line associated with the DRAM memory cell;

forming within the first insulating layer a bit line contact pillar of a contact conductive material extending through the first insulating layer and contacting the drain of the access transistor for electrical connection with a bit line;

forming within the first insulating layer a storage contact pillar of the contact conductive material extending through the first insulating layer and contacting a ground plane region of a memory cell capacitor;

forming within the first insulating layer a ground plate contact pillar composed of the contact conductive material extending through the first insulating layer and contacting a ground plane region of the memory cell capacitor;

forming a trench in the first insulating layer extending down toward the substrate, exposing a portion of the ground plate contact pillar operable as a ground plate of the memory cell capacitor, wherein the ground plate contact pillar resides within the trench formed in the first insulating layer;

depositing a capacitor dielectric layer over the trench, thereby covering the exposed portion of the ground plate contact pillar;

depositing and planarizing a layer of conductive capacitor plate material over the capacitor dielectric layer in the trench, thereby defining a storage plate of the memory cell capacitor;

depositing and planarizing a second insulating layer;

removing portions of the second insulating layer to expose a first opening in the second insulating layer overlying the bit line contact pillar and a second opening overlying the storage contact pillar and a portion of the capacitor plate material used as the storage plate; and

depositing and planarizing a conductive material layer through the openings in the second insulating layer for contact to the bit line contact pillar, the storage contact pillar and a portion of the storage plate, wherein the conductive material within the second opening comprises an electrical connection between the source of the access transistor and the storage plate of the capacitor structure.

48. The method of claim 47, wherein the forming a trench in the first insulating layer extends down to about the uppermost surface of the substrate.

49. An integrated circuit comprising:

a dielectric layer disposed between a substrate and a first metal layer;

a trench defined by a recess in the dielectric layer;

a first contact pillar extending substantially from a top surface of the substrate to a bottom surface of the first metal layer within the trench; and

a capacitor formed in the trench overlying the first contact pillar such that the capacitor is formed at least in part on a side of the first contact pillar.

50. The integrated circuit of claim 49, further comprising a second contact pillar extending substantially from the top surface of the substrate to a bottom surface of another portion of the first metal layer, wherein the second contact pillar is substantially the same height as the first contact pillar.

51. The integrated circuit of claim 49, wherein the capacitor comprises a storage element of a memory cell.

52. The integrated circuit of claim 51, wherein a storage node of the storage element comprises the first contact pillar.

53. The integrated circuit of claim 52, wherein the storage node further comprises a conducting layer lining the trench and the side of the first contact pillar.